RECEIVED
CENTRAL FAX CENTER
FEB 25 2008

Customer No.: 31561
Application No.: 10/709,848
Docket No.: 12877-US-PA

AMENDMENT

To the Claims:

Please amend the claims as follows:

Claims 1-23. (canceled).

Claim 24. (previously presented) A source driver, receiving a master/slave setting signal, a clock signal, a display data, and a control signal to drive a display panel, comprising:

a receiver for receiving said clock signal, said display data, and said control signal; and

a transmitter, coupled to said receiver, transmitter receiving said master/slave setting signal, said transmitter responsive to said master/slave setting signal operating in one of a master mode and a slave mode; wherein when said transmitter operates in said master mode, said transmitter enhances a driving ability of said clock signal, said display data, and said control signal for use of another source driver in a next stage; when said transmitter operates in said slave mode, said transmitter directly outputs said clock signal, said display data, and said control signal received from said receiver for use of said another source driver in said next stage.

Claim 25. (original) The source driver of claim 24, wherein said transmitter is a

differential signal transmitter.

Claim 26. (original) The source driver of claim 25, wherein said receiver is a differential signal receiver.

Claim 27. (original) The source driver of claim 25, wherein said transmitter is a voltage mode differential signal transmitter.

Claim 28. (original) The source driver of claim 25, wherein said transmitter is a current mode differential signal transmitter.

Claim 29. (original) The source driver of claim 24, wherein said transmitter is a TTL signal transmitter.

Claim 30. (original) The source driver of claim 29, wherein said receiver is a TTL signal receiver.

Claim 31. (previously presented) The source driver of claim 24, wherein said transmitter includes:

a data synchronization circuit synchronizing said clock signal, said display data, and said control signal received from said receiver; and

a plurality of buffers, coupled to said data synchronization circuit, receiving said synchronized clock signal, said synchronized display data, and said synchronized control signal, enhancing said driving ability of said synchronized clock signal, said synchronized display data, and said synchronized control signal for use of said another source driver in said next stage.

Claim 32. (previously presented) The source driver of claim 24, wherein said transmitter includes a plurality of voltage buffers receiving said clock signal, said display data, and said control signal, enhancing said driving ability of said clock signal, said display data, and said control signal for use of said another source driver in said next stage.

Claim 33 (original) The source driver of claim 24, wherein said display panel is a α-Si liquid crystal display panel.

Claim 34 (original) The source driver of claim 24, wherein said display panel is a low temperature poly-silicon liquid crystal display panel.

Claim 35 (currently amended) A flat panel display, comprising:

a display panel;

a timing controller outputting a clock signal, a display data, and a control signal;

a control circuit outputting a plurality of mater/slave setting signals; and

a plurality of source drivers, said plurality of source drivers being series-connected to be a series structure, said plurality of source drivers being coupled to said display panel, one end of said series structure being coupled to said timing controller, said plurality of source drivers receiving said clock signal, said display data, and said control signal to drive said display panel, each of said plurality of source drivers responsive to a corresponding one of said plurality of mater/slave setting signals determining whether to enhance a driving ability of said clock signal, said display data, and said control signal for use of another source driver in a next stage, wherein each of said plurality of source drivers comprises:

a receiver for receiving said clock signal, said display data, and said control signal; and

a transmitter, coupled to said receiver, transmitter receiving said master/slave setting signal, said transmitter responsive to said master/slave setting signal operating in one of a master mode and a slave mode; wherein when said transmitter operates in said master mode, said transmitter enhances said driving ability of said clock signal, said display data, and said control signal for use of said another source driver in said next stage; when said transmitter operates in said slave mode, said transmitter directly outputs said clock signal, said display data, and said control signal received from said receiver for use of said another source driver in said next stage.

Claim 36. (canceled)

Claim 37. (currently amended) The flat panel display of claim [[36]]35, wherein said transmitter is a differential signal transmitter.

Claim 38. (original) The flat panel display of claim 37, wherein said receiver is a differential signal receiver.

Claim 39. (original) The flat panel display of claim 37, wherein said transmitter is a voltage mode differential signal transmitter.

Claim 40. (original) The flat panel display of claim 37, wherein said transmitter is a current mode differential signal transmitter.

Claim 41. (currently amended) The flat panel display of claim [[36]]35, wherein said transmitter is a TTL signal transmitter.

Claim 42. (original) The flat panel display of claim 41, wherein said receiver is a TTL signal receiver.

Claim 43. (currently amended) The flat panel display of claim [[36]]35, wherein said transmitter includes:

a data synchronization circuit synchronizing said clock signal, said display data, and said control signal received from said receiver; and

a plurality of buffers, coupled to said data synchronization circuit, receiving said synchronized clock signal, said synchronized display data, and said synchronized control signal, enhancing said driving ability of said synchronized clock signal, said synchronized display data, and said synchronized control signal for use of said another source driver in said next stage.

Claim 44. (currently amended) The flat panel display of claim [[36]]35, wherein said transmitter includes a plurality of voltage buffers receiving said clock signal, said display data, and said control signal, enhancing said driving ability of said clock signal, said display data, and said control signal for use of said another source driver in said next stage.

Claim 45. (original) The flat panel display of claim 35, wherein said display panel is a α-Si liquid crystal display panel.

Claim 46. (original) The flat panel display of claim 35, wherein said display panel is a low temperature poly-silicon liquid crystal display panel.